Detector R&D for NSLS-II

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NSLS

Outline

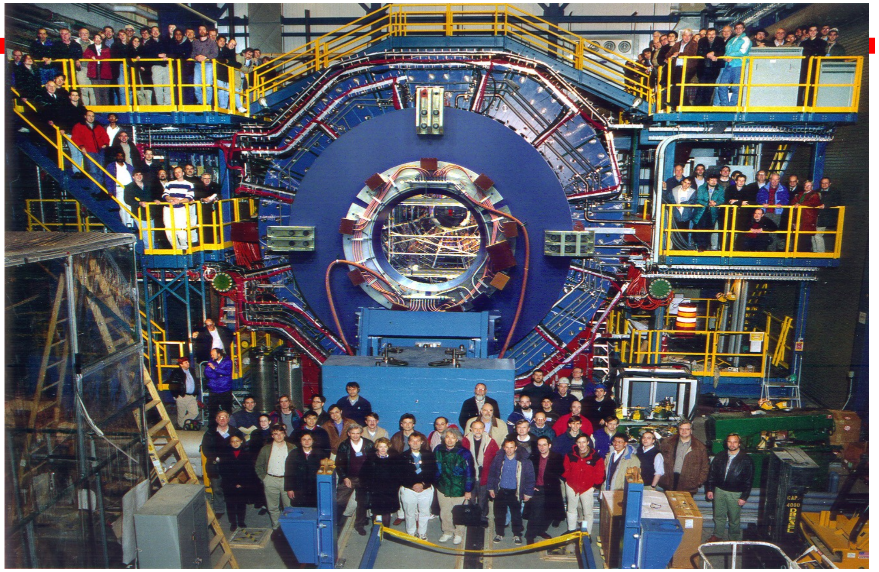
- NSLS-II detector R&D
- Cultural issues
- Silicon detectors
- NSLS Detectors
- LCLS detectors
- Emerging Technologies for Sensor/ASIC Integration
- Requirements for NSLS-II Detectors
- Proposed R&D Plan

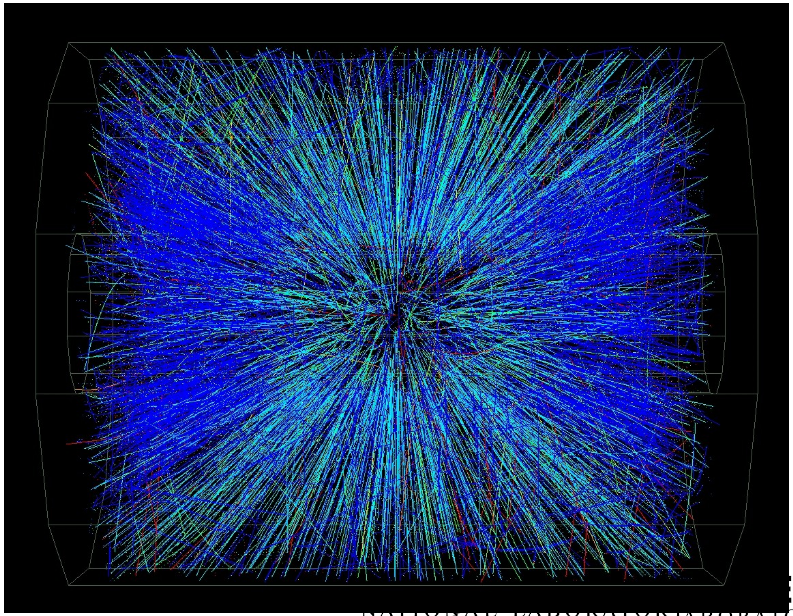
Detector R&D for XPCS

- NSLS-II does not have a detector R&D program
  - Any R&D will be independently funded
  - FY08 budget will not allow any new R&D
- No optimal detector exists for XPCS
  - Need to develop a new, **REVOLUTIONARY** class of detector
  - Significant computation 'on-pixel'
  - Potentially viable technology under development (ILC R&D, IT industry)
- LCLS detectors will be useful at millisecond timescales

Culture

- SR and HEP are cultural opposites
  - HEP: teams of hundreds for one experiment, complex detector system
  - SR: teams of <10 usually, simple apparatus.
  - HEP: Experiment takes years
  - SR: Experiment takes hours or days
  - HEP: Detector IS experiment
    - Scientists closely involved in design
  - SR: SAMPLE is experiment: SR and detector a necessary evil
    - Scientists just want the result





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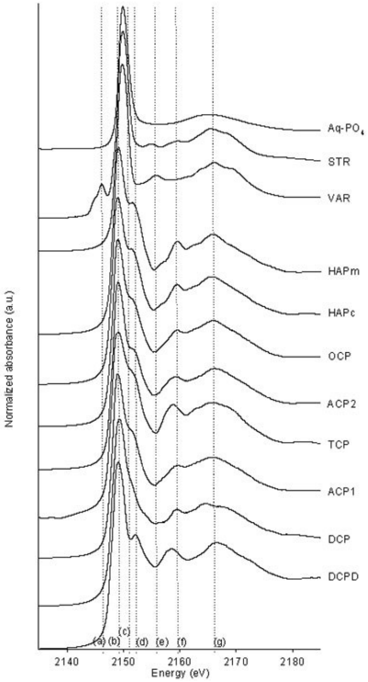
Sato, Solomon, Hyland, Keterings, Lehmann, Cornell Univ. 2006

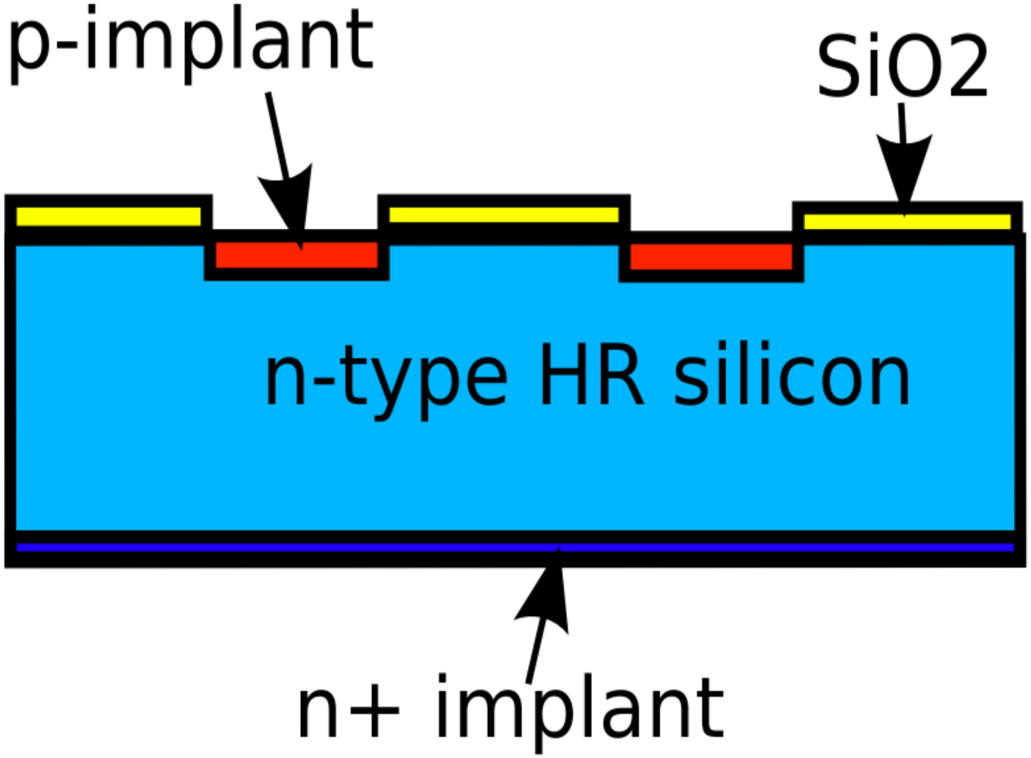


What is the ideal XPCS detector?

- Specifications:
  - 1 micron pixels
  - 1000 megapixels
  - 1ns time resolution
  - 100% efficient at all energies
  - Free
- Various physical and fiscal realities conspire to prevent this being realized.
- Photon-counting provides best S/N.

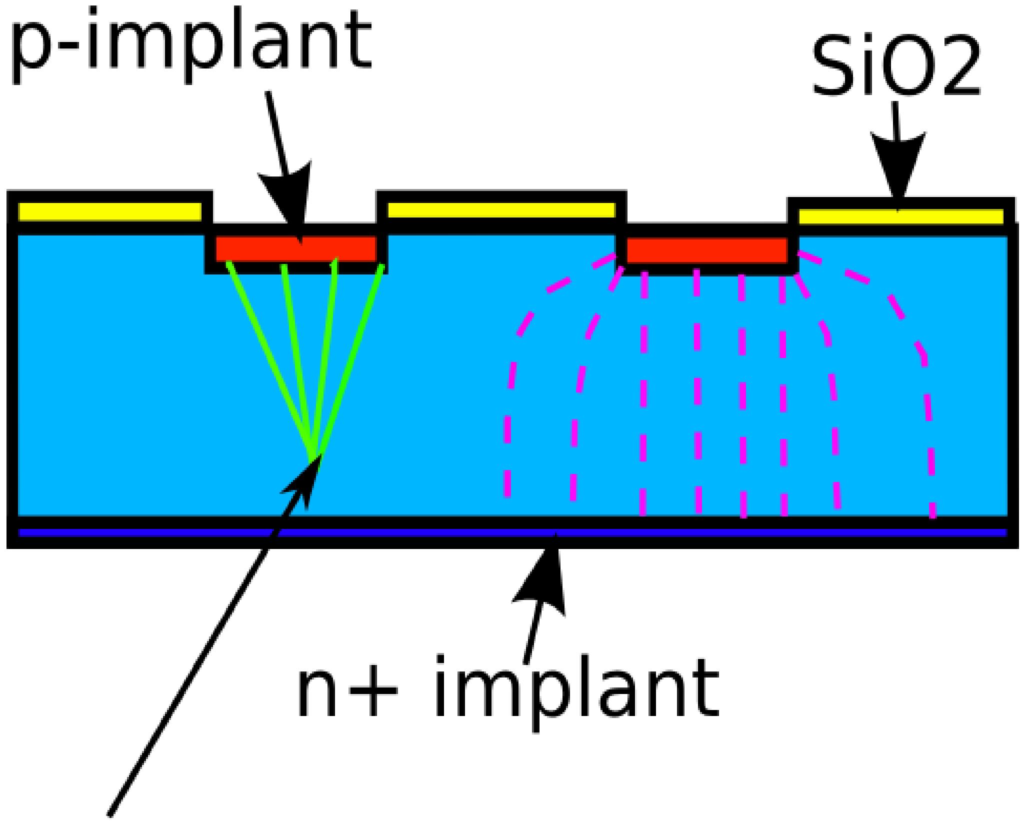
Simplest silicon detector

- vertical P-N Junction
- Wafer bulk is active (unlike commercial CMOS)
- Wafer must be very high resitivity (>5kohm-cm) to allow full depletion
- SiO2 provides electrical isolation between adjacent diodes

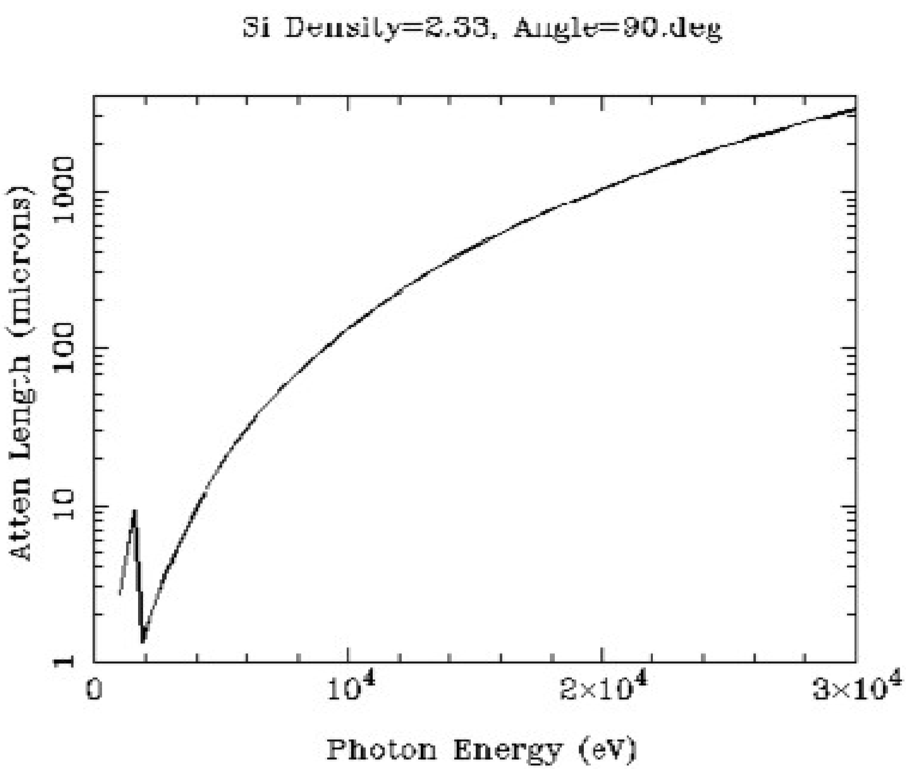


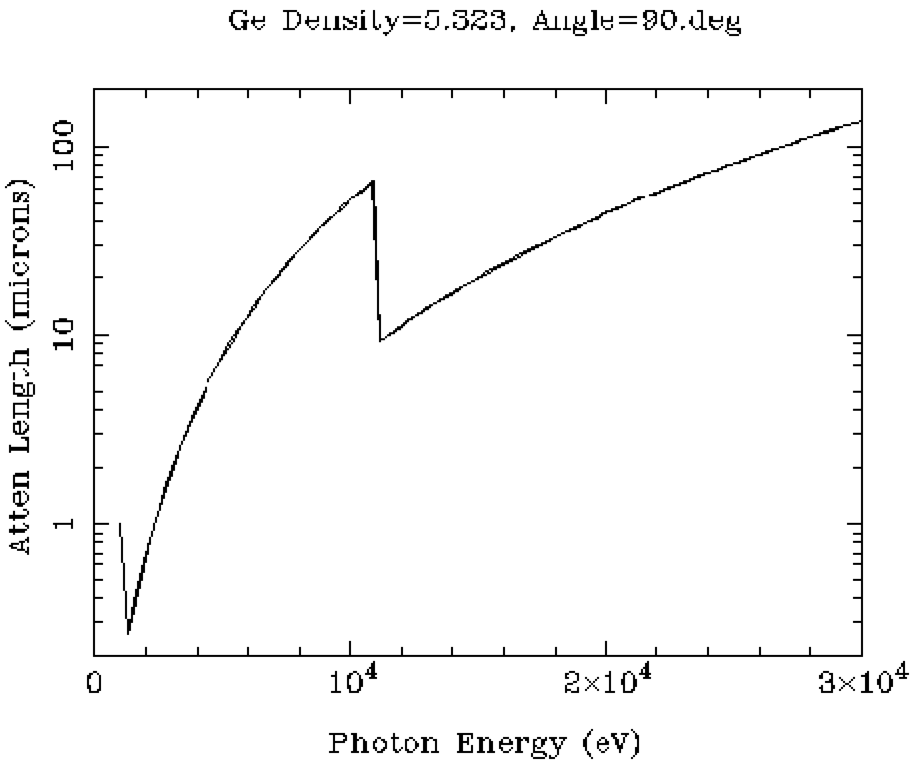
Internal fields and trajectories

- Photon produces e-h pairs.
- charges drift towards surfaces due to bias field (wafer fully depleted). Takes about 20ns for 0.4mm wafer.
- Transverse momentum of charges causes charge spreading
- For 10keV photon, spreading is 20-30um for 0.4mm wafer.
- **SMALL PIXELS WILL PERFORM POORLY** as photon-counting detectors.



Absorption length for Si & Ge





- Materials science needs E > 20keV to penetrate dense materials (alloys, ceramics etc.)

- Biology needs higher E to reduce radiation damage

NSLS Detectors

- A series of detectors for selected SR applications has been developed over the past ~5 years
- Key technologies:
  - Silicon pad and strip detectors (Inst. Div.)
  - CMOS ASICs (Inst. Div.)
  - System design, packaging, fixturing, DAQ (NSLS)
- Significant performance advantages due to the ability to utilize highly parallel architectures

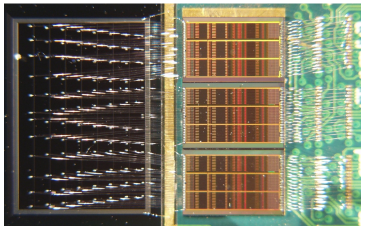
The MAIA Project

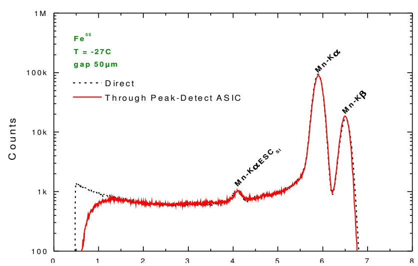
Si pad sensor

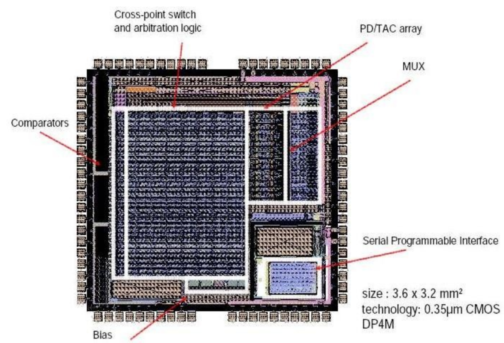
preamp/shaper ASIC

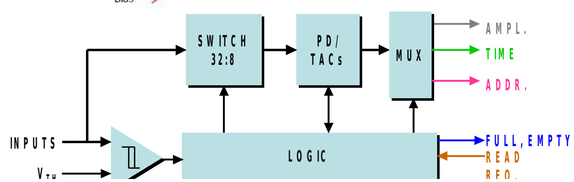
Peak detector – derandomizer - multiplexer ASIC

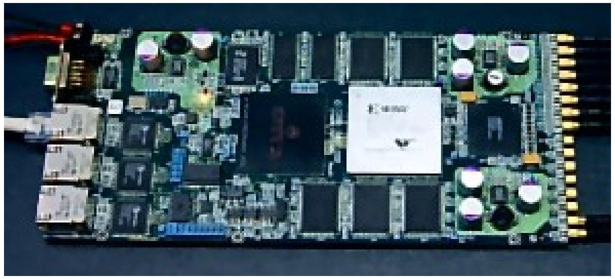
pipelined, parallel processor and digitizer









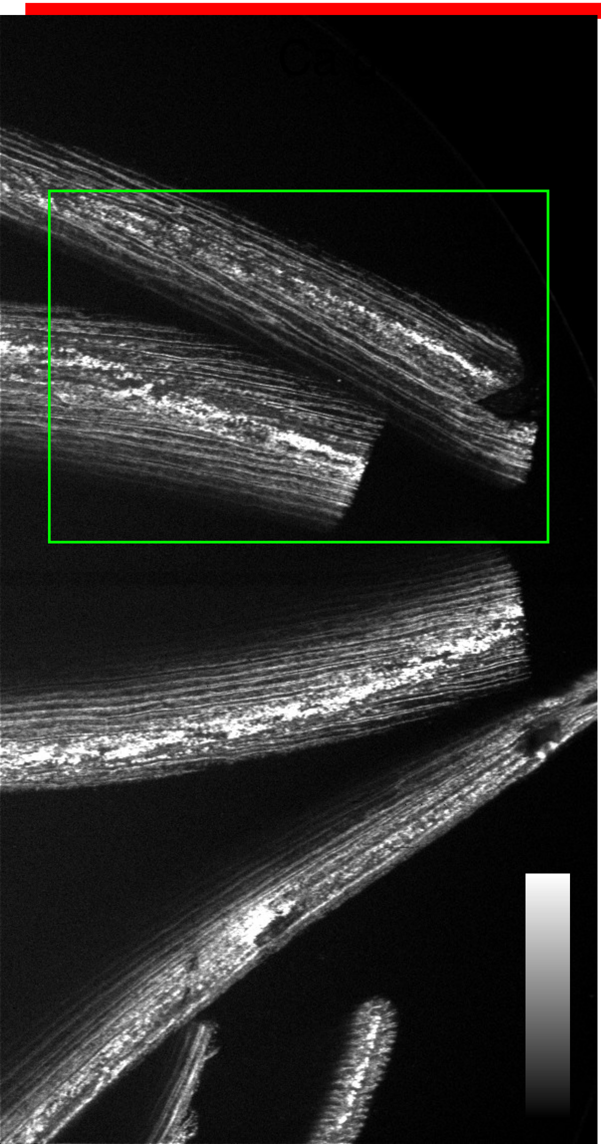


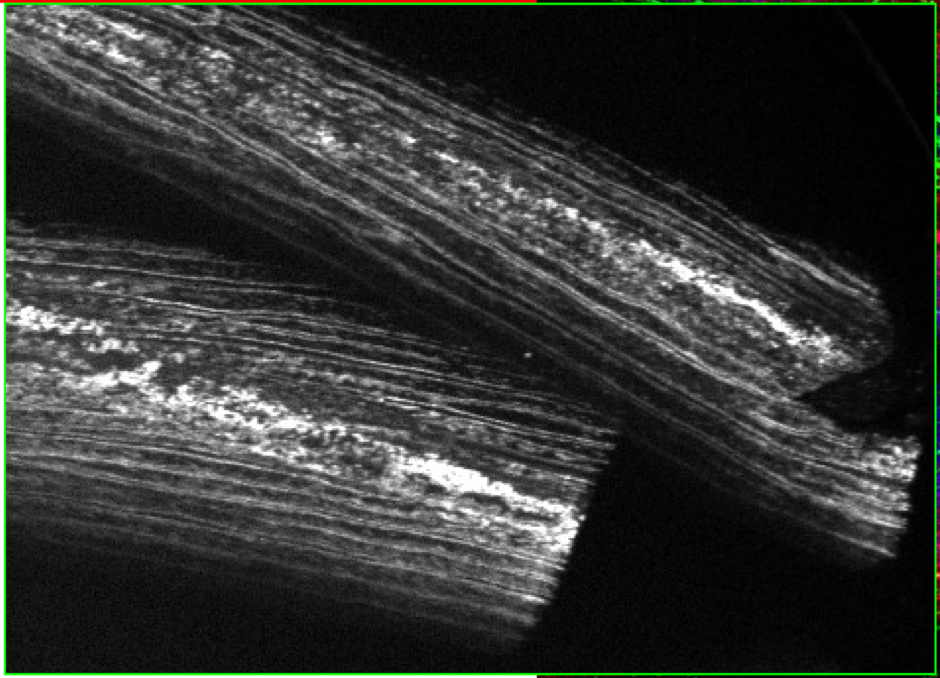
- ***Preamp/shaper ASIC*** achieves 184eV resolution (Mn Kα).
- 32-channel peak detecting derandomizer and multiplexer with time-over-threshold for pileup rejection or arrival time for XPCS.
- ***Dynamic Analysis*** method demonstrated for imaging of SXRF data at X27A.
- DA real-time spectral deconvolution demonstrated at ***10^8 events/second*** using HYMOD.
- FPGA could be programmed to perform autocorrellation in real time.

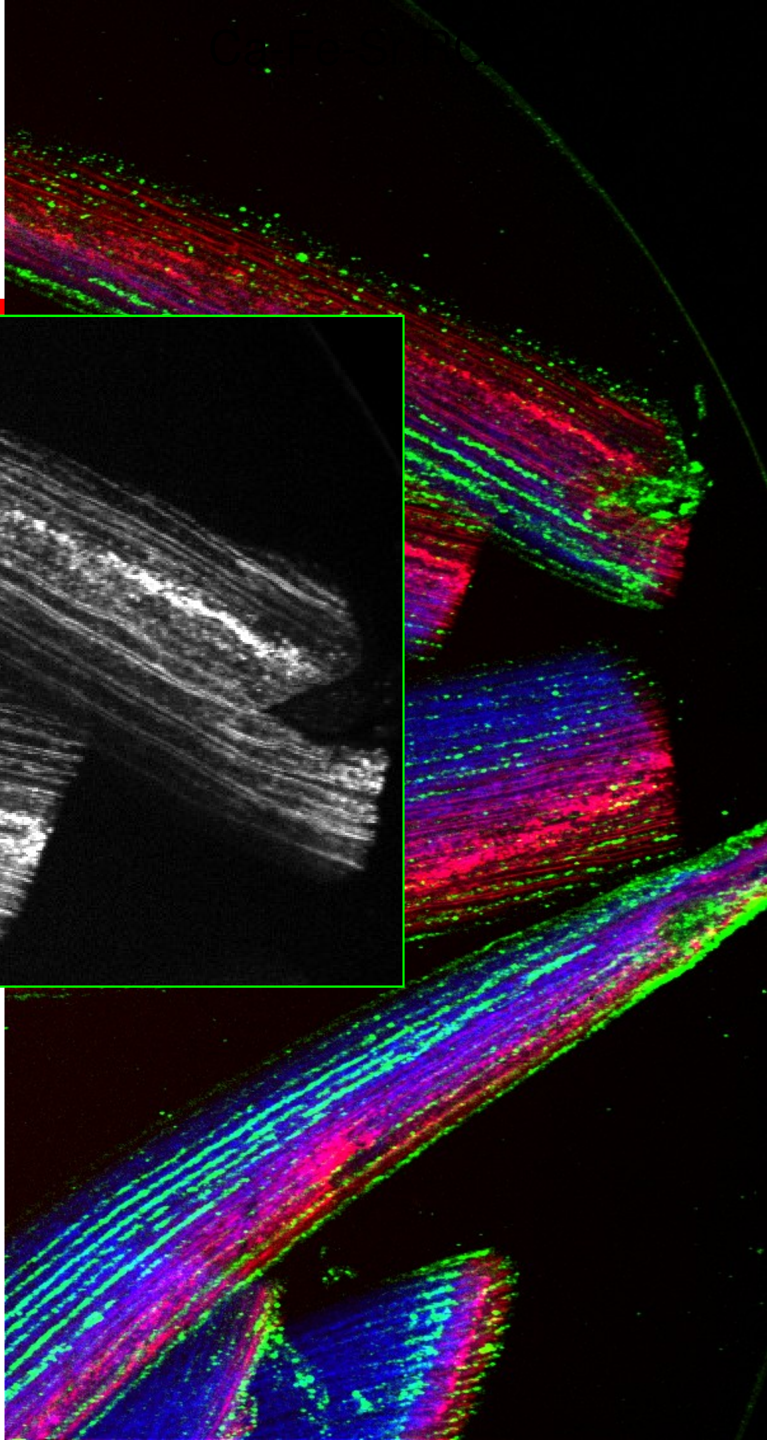
Tests of the Maia-96 system

Some examples from NSLS **September 2007 experiment**

Long run (#295): Acacia stems, Western Australia







1200 x 2267 (9 x 17 mm²)
5.7 hours (7.5 ms dwell)
7.5 x 7.5 μm² pixels

Tests of the Maia-96 system

Some examples from NSLS **September 2007 experiment**

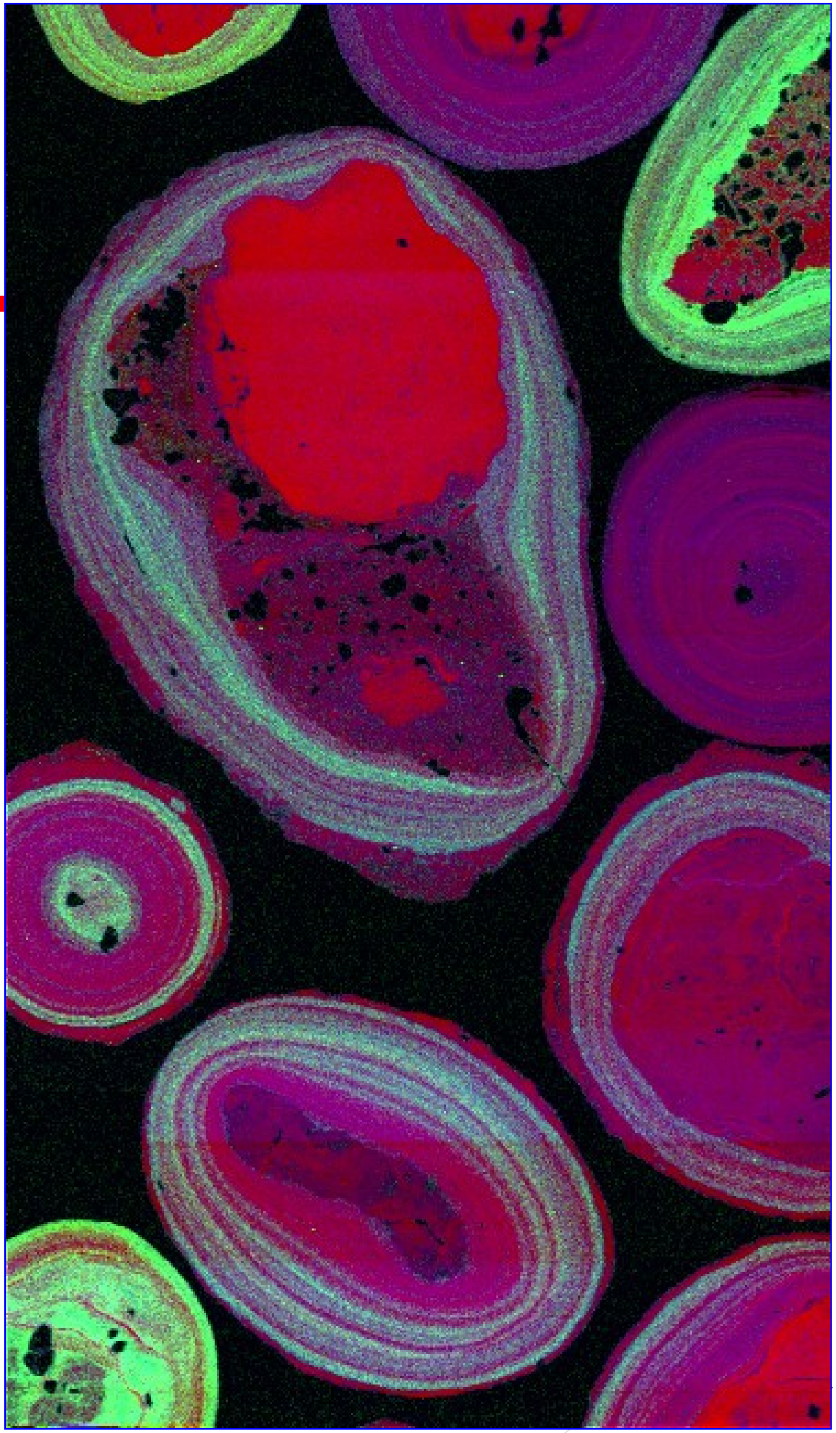
Long run (#204): Iron-oxide nodules, Rose Dam, WA

1625 x 2625 pixels (13 x 21 mm^2)

6.3 hours (**5 ms dwell** per pixel)

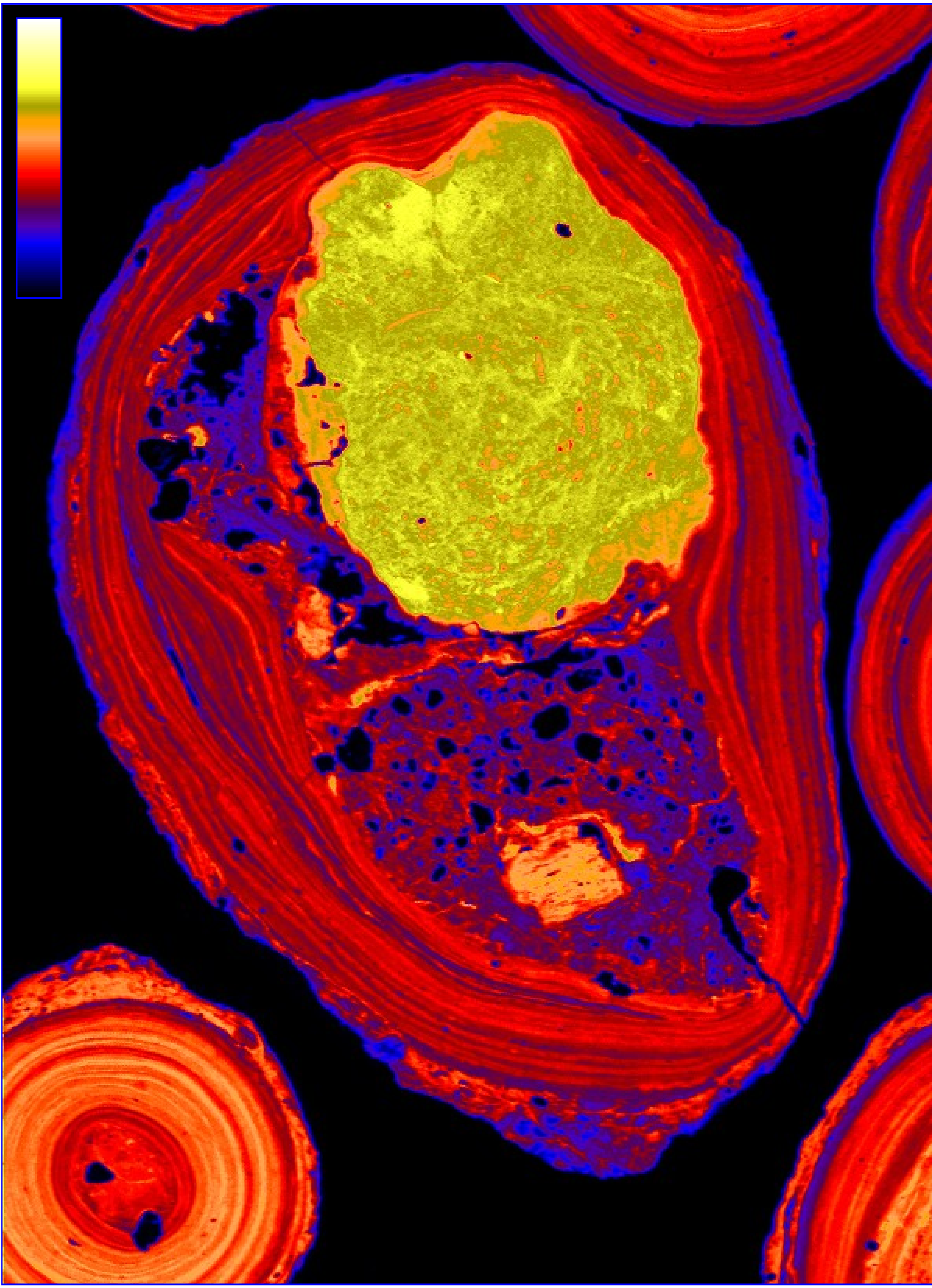
7.5 x 7.5 μm^2 pixels

0-2 MHz count rates → good image counting statistics



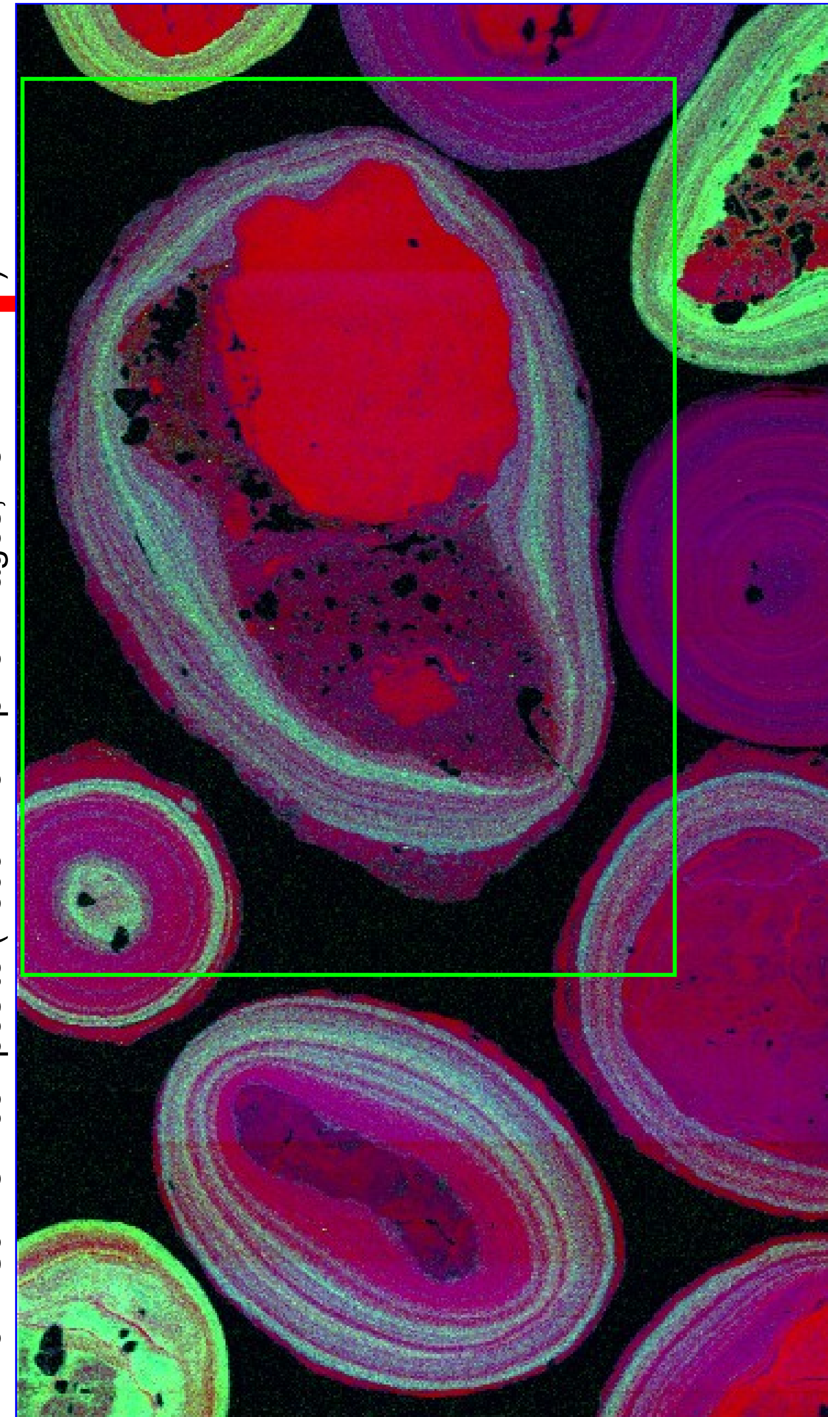
Fe-Y-Cu RGB composite

Tests of the Maia-96 system



Iron oxide nodules, Rose Dam WA

Fe-Y-Cu RGB composite (1500 x 2624 pixel images, 13 x 21 mm^2)

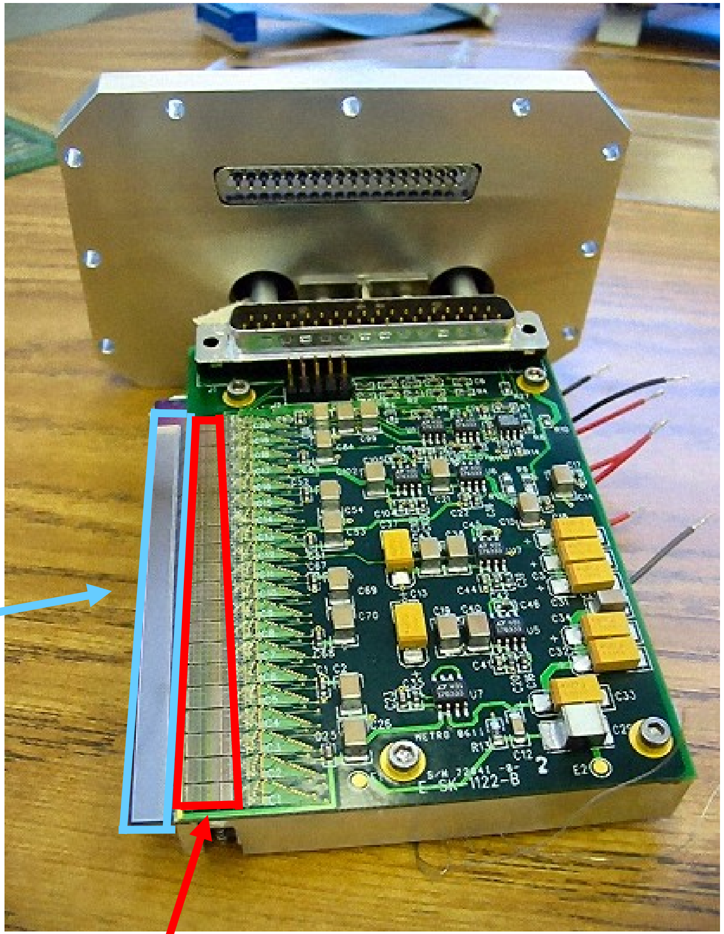


Application to XPCS?

- Each photon can be time-stamped to sub-microsecond accuracy
- Each photon is labelled with its energy and detector number
- Analysis of this 'list-mode' data can yield correlations, possibly in real time.
- Is this useful?
  - Relatively few pixels (~1000)
  - large pixels (1mm^2)
  - Good time resolution (microseconds)
- Can use pinhole array to determine effective pixel size
  - Just lose coverage; add more detectors!

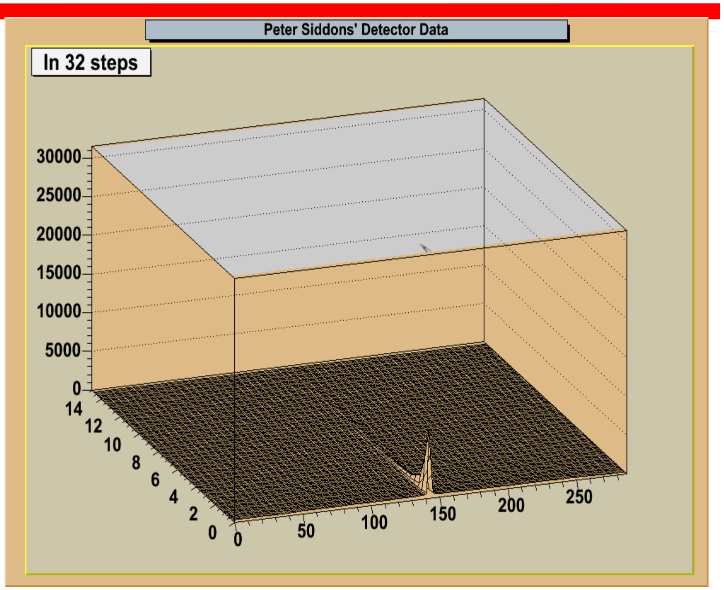
Detector for Diffraction Applications

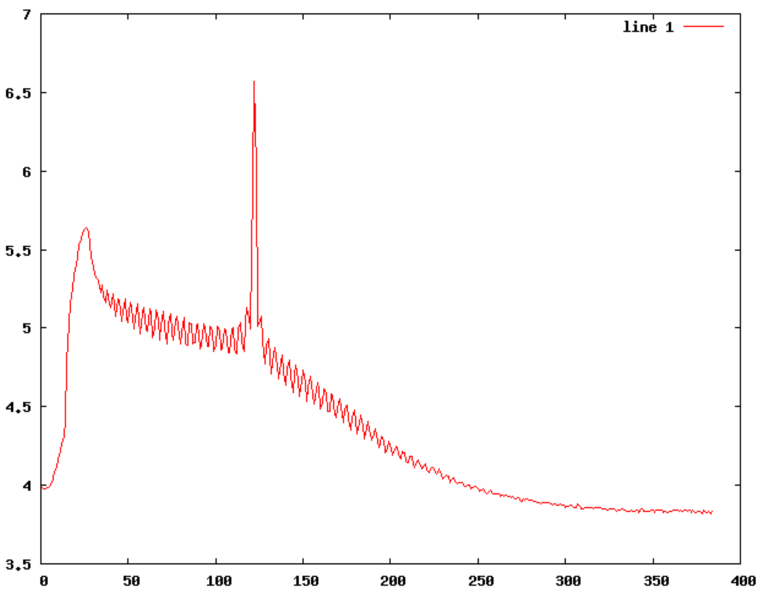
- 80mm long silicon PSD
- 640 channels, ASIC readout
- 125um pitch
- 4mm wide
- 0.4mm thick
- 350eV energy resolution @ 5.9keV



Application Examples

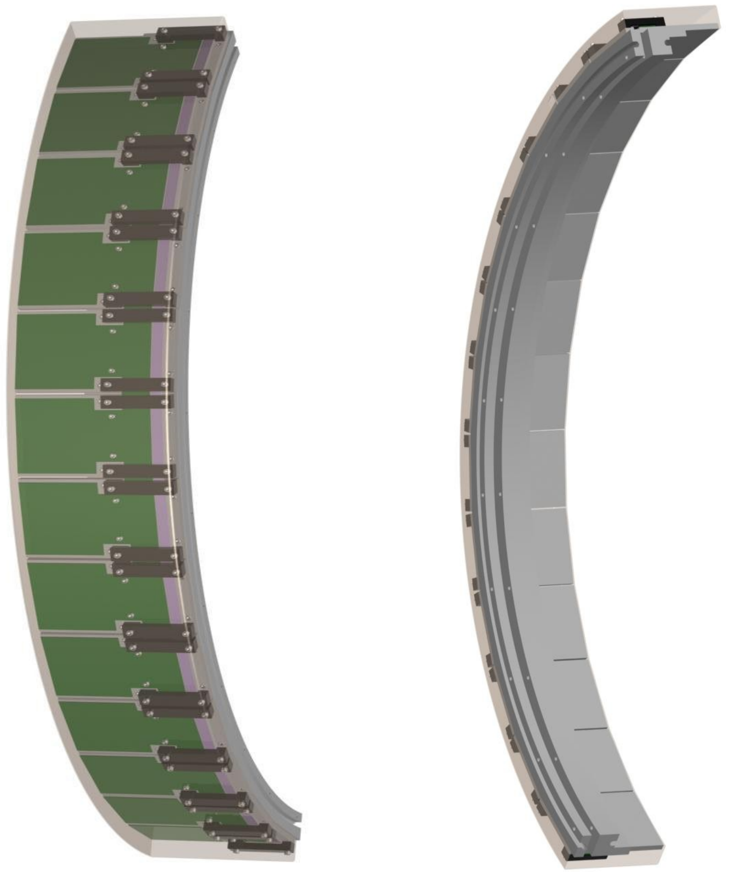
- Real-time growth / surface modification
  - *Beamline X21 in-situ growth endstation*
  - *Several high-impact pubs*
- Reflectivity / truncation rods / GISAXS
  - *Tests at Cornell and APS (COBRA studies)*
  - *System delivered for X9 undulator/CFN*
- Powder diffraction
  - *Detectors in use at X16C, X14A*
- Inelastic scattering
  - *System delivered to Argonne*
  - *x10 intensity, x2 resolution on MERIX*
  - *Collaboration with Taiwan NSRRC*
- *Lots of interest*
  - *Cornell*
  - *Other APS*
  - *SSRL*





Large array for NSLS

- 120 degrees
- ~7000 channels
- 0.014 deg. Resolution
- ~1ms readout time
- ~350eV energy resolution



LCLS detectors

LCLS is a Free-Electron Laser x-ray source being built at SLAC (Stanford). It will produce <100fs long x-ray pulses at 120Hz.

BNL is contracted to supply fast readout Imaging detectors

They must:

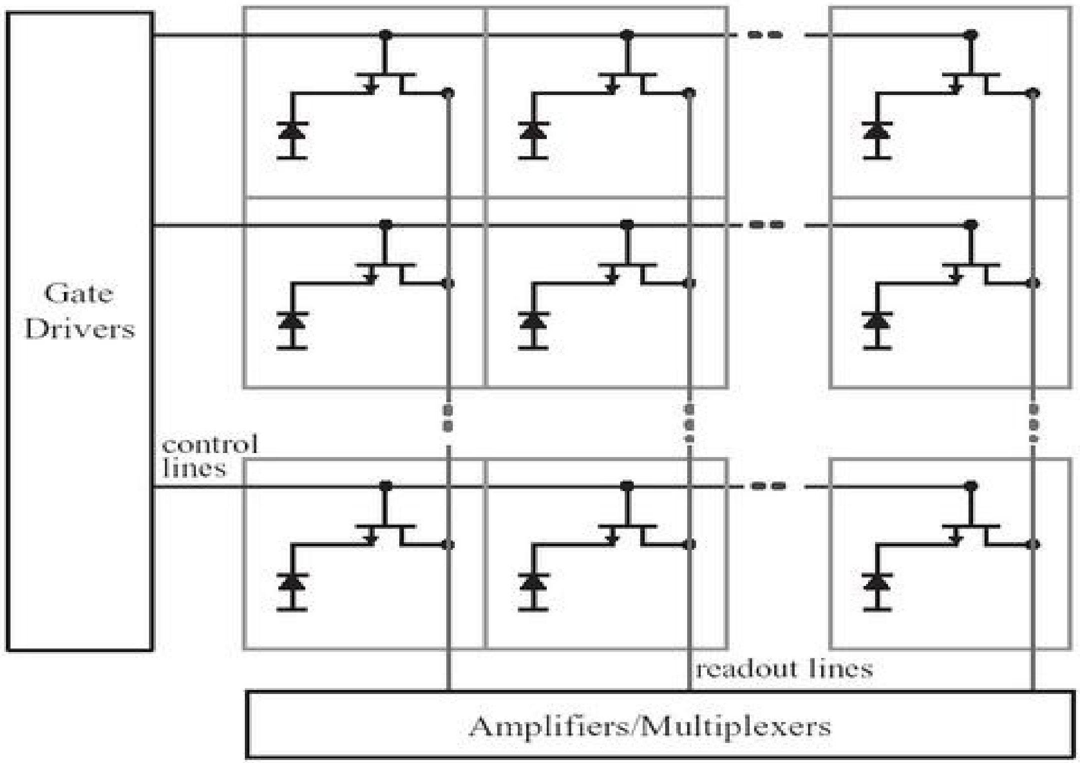
- Be integrating detectors because of LCLS time structure
- Have large dynamic range for single-shot experiments
- Have low noise
- Have < 8ms readout time

These detectors will also be valuable at a storage ring

They will be useful for XPCS at millisecond timescales

Active matrix readout

- **Charge stored in diode capacitance (switches off)**
- **Readout amplifier on each column**
- **Each ADC reads 16 columns (multiplexed)**
- **Switches turned on sequentially row-by-row**
- **Charge read out and digitized**
- **1us per row => 1ms for 1000 rows.**
  - 8-channel 40MHz/channel ADC chip
  - 8 chips, each ADC multiplexed among 16 columns
- **2Gb/s data rate**



Readout system

Row-by-row readout, 1us/row

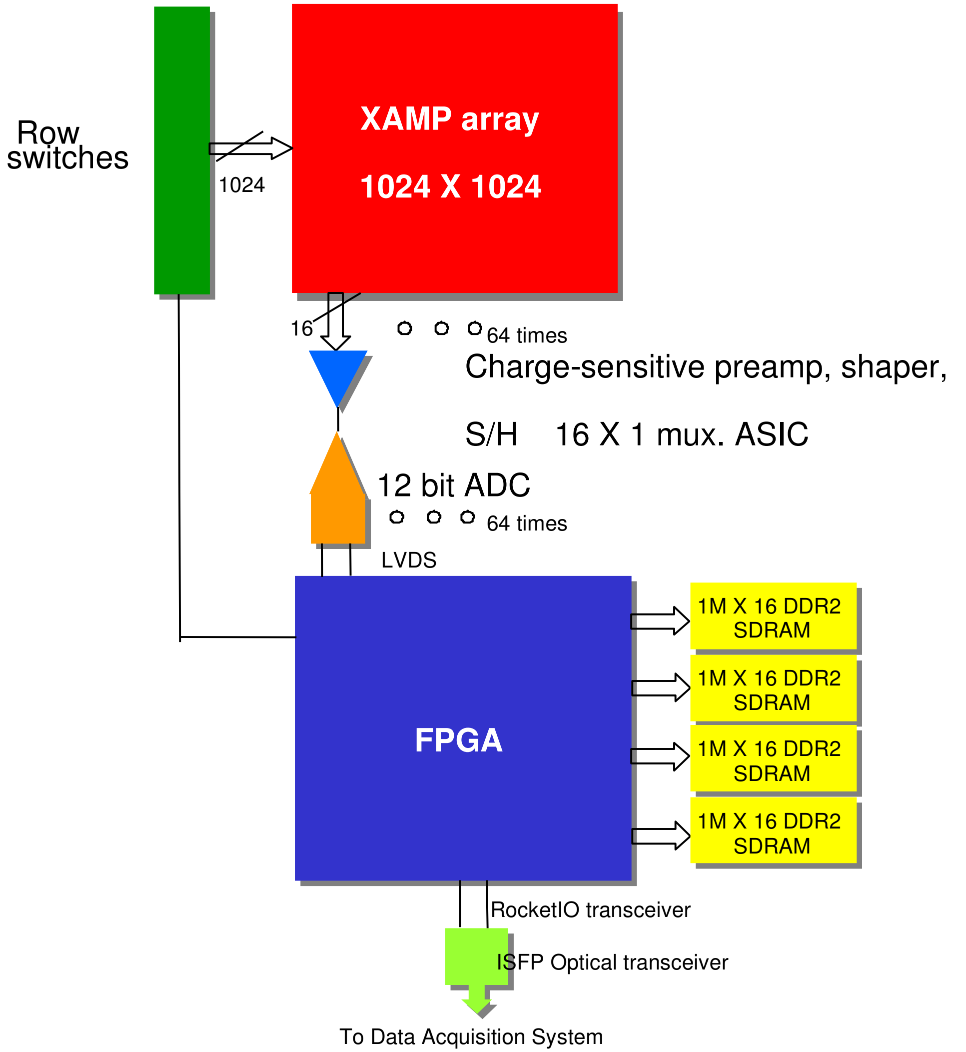
8 Fast (>20MHz) 8-channel ADC's multiplexed e.g. x16 columns = 1024

2GB/s instantaneous raw data from ADCs

250MB/s averaged, i.e. to be stored, based on 120Hz cycle. More if rep. rate is upgraded.

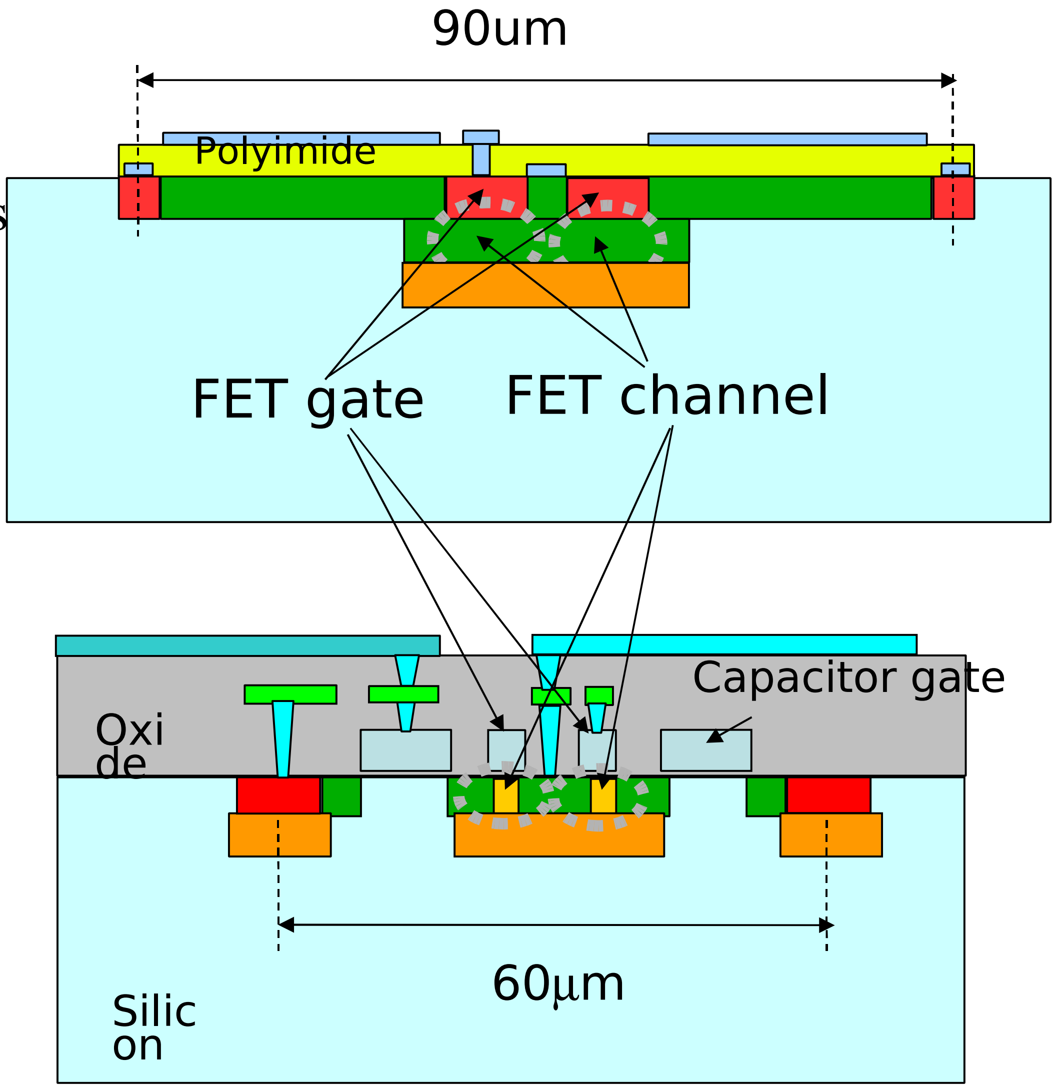
Data streamed through FPGA to fast memory and terabyte disk store.

- FPGA does background correction



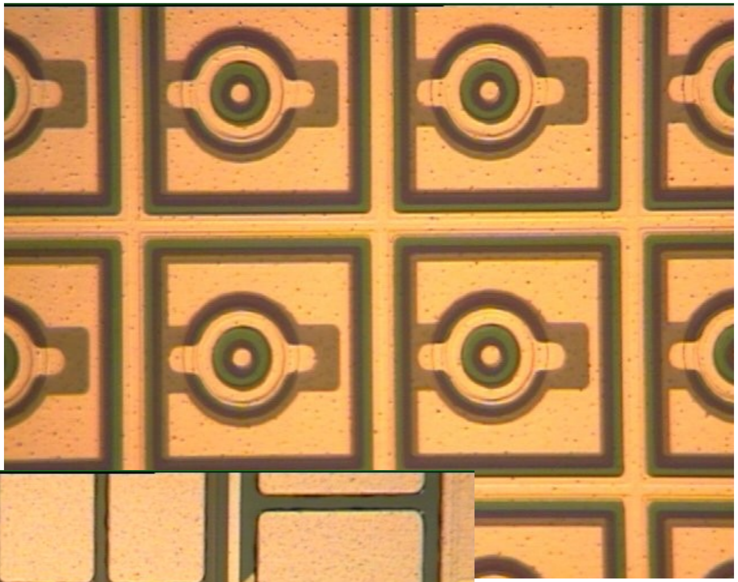
JFET vs MOSFET structure comparison

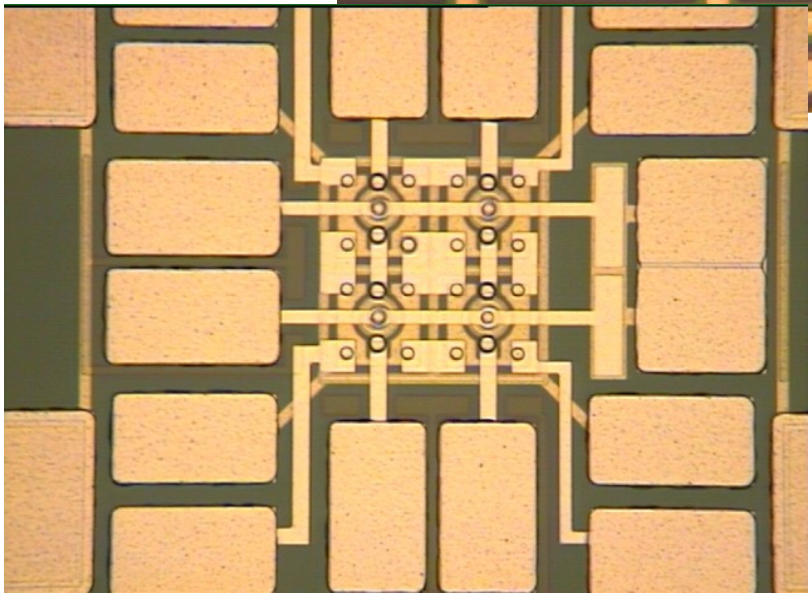
- Both start with high-res. wafer..
- Both make implants on both sides of the wafer
- BNL's process needs careful alignment between layers
- IBM's process is self-aligning for several key layers
- If successful, IBM's process allows more complex circuits to be designed than BNL's
- We have first devices from both processes in hand.



Images of BNL matrix structures

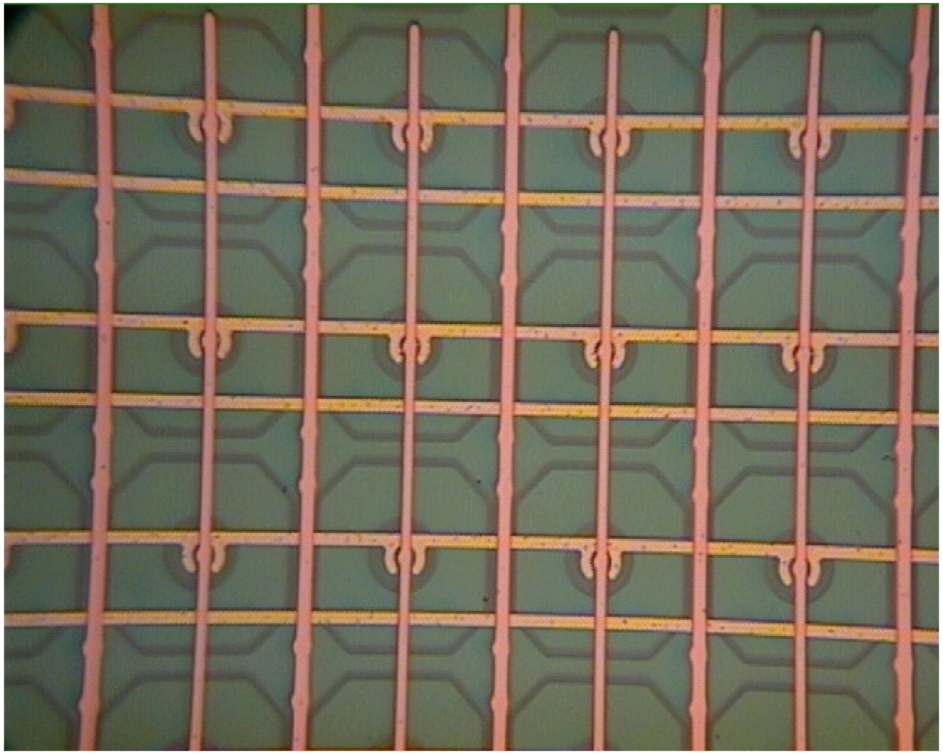
- Upper picture shows gate ring metal and charge collection capacitor plate
- Lower picture shows complete 2 x 2 array, showing two metal layers separated by a polyimide insulation layer.



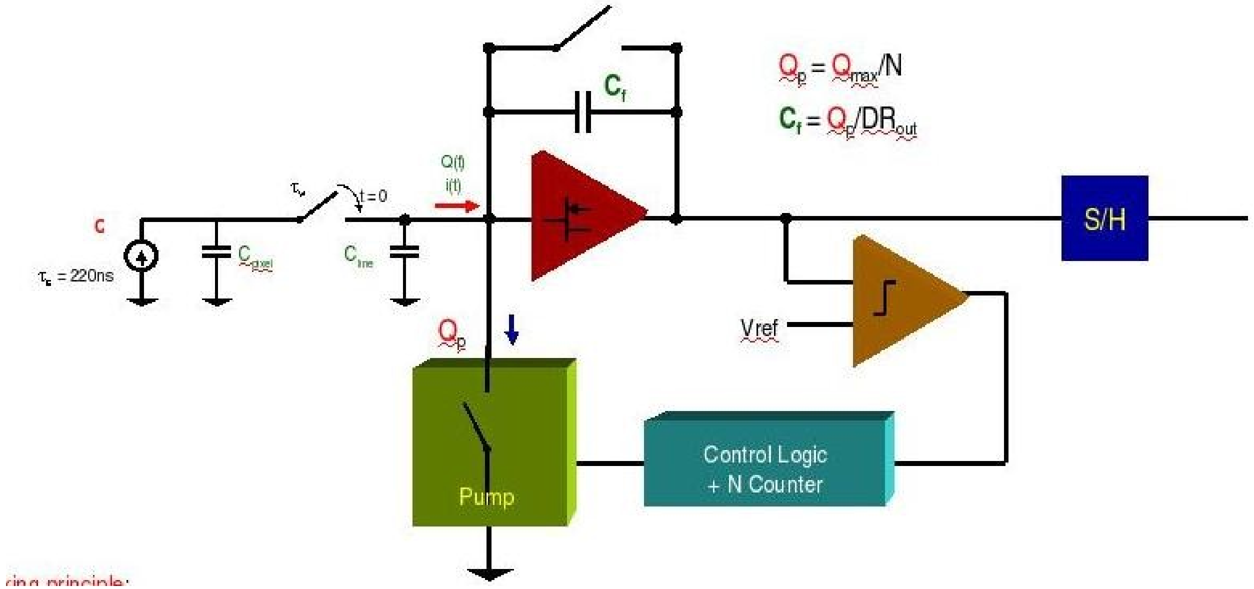


IBM collaboration

- MOS version of XAMPS
- Fabricated to our design by IBM Yorktown Heights
- Potentially lower noise
- Potentially mass-produceable



Readout ASIC



- Problem is to handle both large signals and small signals while maintaining low noise for small signals
- Circuit works by 'pumping' large charge packets out of integrator summing node until amplfier falls into linear operation, then digitizing remainder.

The future

- Need to find a technology to put more functionality in each pixel
- Requirements for fabricating circuits are different from those for fabricating sensors
- How can we integrate these divergent requirements?

Possible Monolithic Approaches for Sensor/ASIC Integration

- Problem: sensor and readout optimize differently
- Solutions:
- Existing Technology
  - sensor in CMOS process (MAPS)
  - transistor in sensor process (DEPFET, XAMPS)
- Charge-Shifting
  - capture charge in a potential well and physically move it to output port (CCD, CDD)
- Physical Connection
  - bump bonding (PbSn, In)
  - direct wafer-wafer bonding

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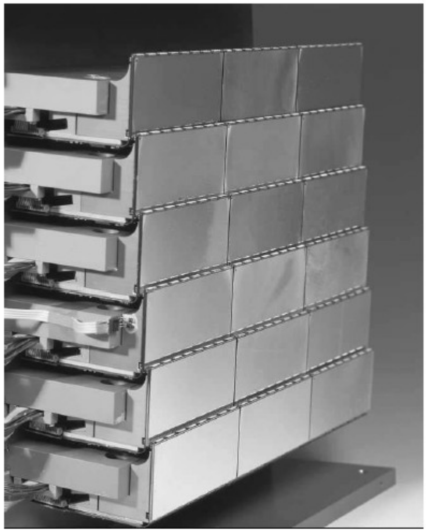
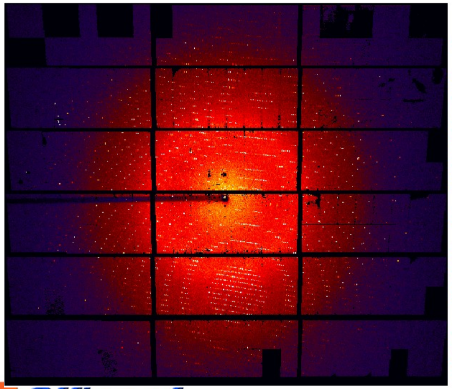
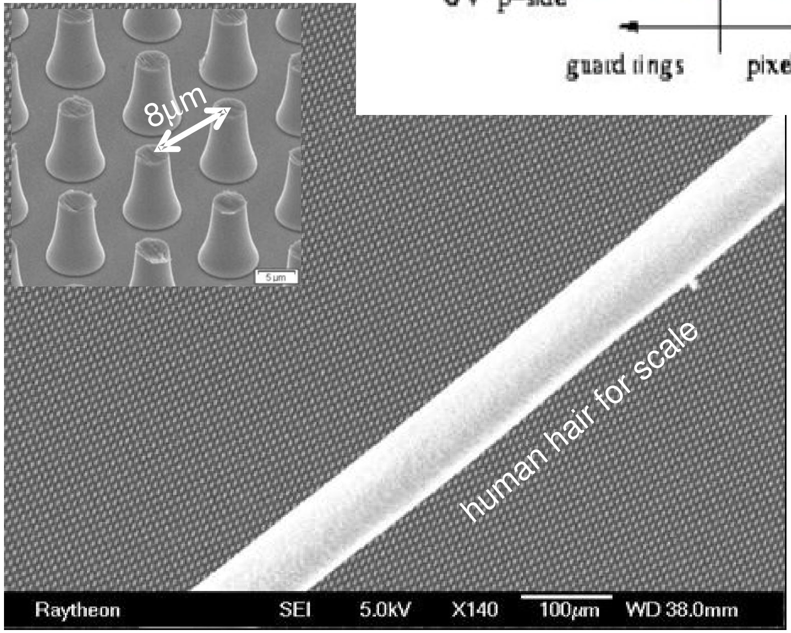
Bump-bonding: Examples

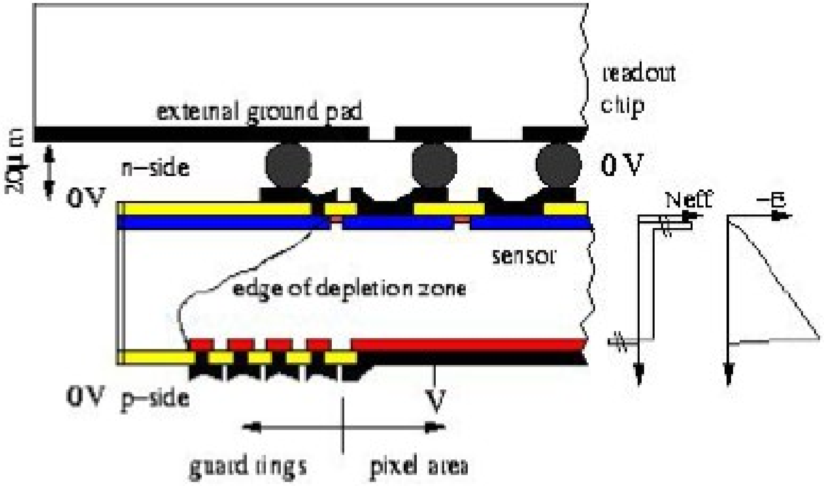


PILATUS 1M

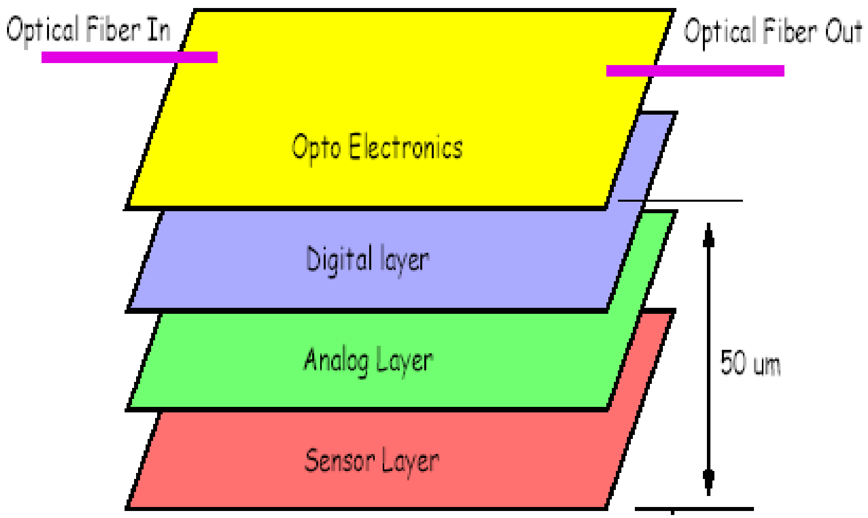
Swiss Light Source



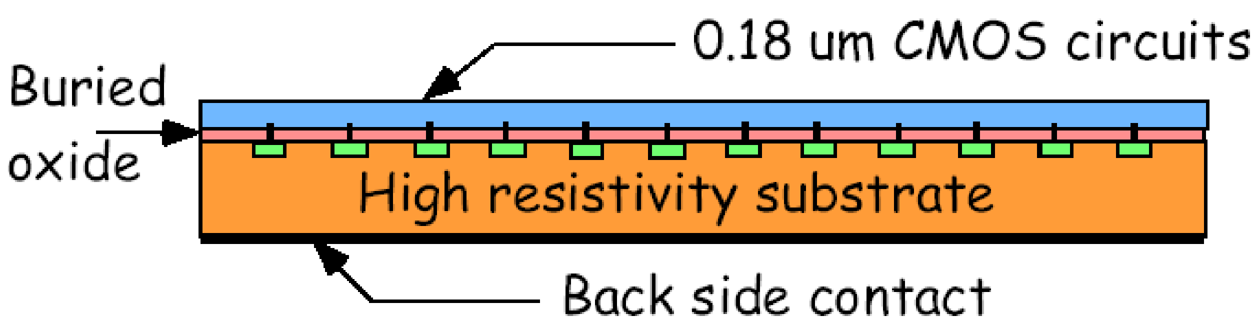




direct wafer-wafer bonding

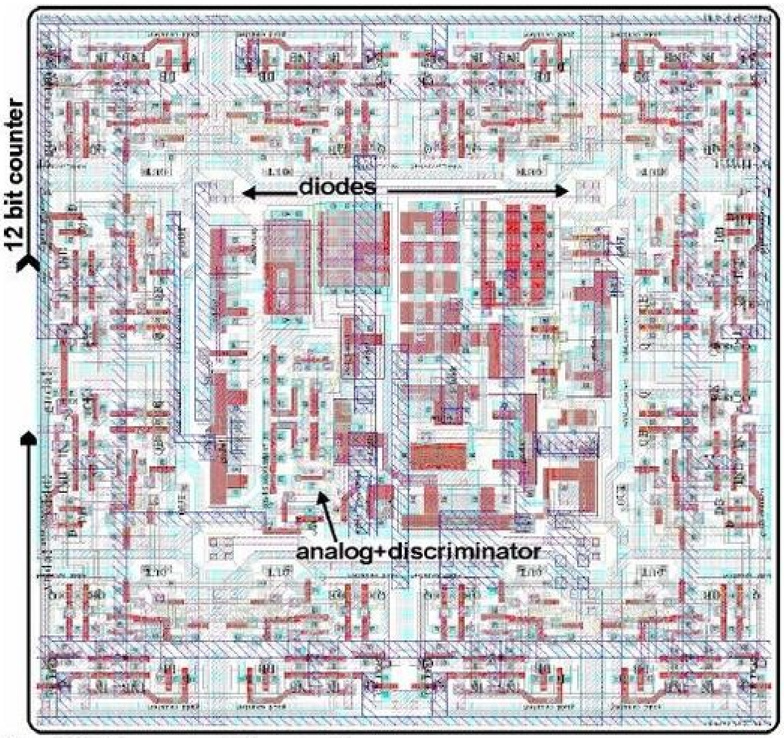


- Ultimate goal is monolithic integration of any technology
- Immediate push in industry is for reducing wireload distribution in digital ICs
- Science applications being pursued in optical/IR imaging, HEP tracking
- FNAL and KEK have active HEP designs
- Processes available at Lincoln Labs, JPL, OKI Semiconductor, IBM (?)



A Monolithic Photon-counting pixel detector

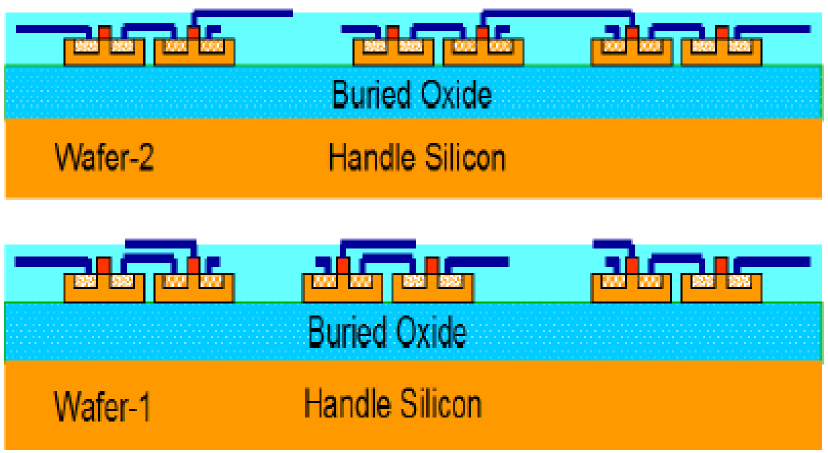
- 26 x 26 um (G. Deptuch, 2006)
  - 280 transistors
  - Built using standard SOI CMOS
  - Impossible to properly prepare 'detector'.
- Bonding CMOS and sensor after sensor implant gives full control over interfaces
- 60 x 60 um pixel would allow ~1500 transistors
  - Better analog circuits
  - More bits
  - Double-buffering (no dead-time for readout?)



Process flow for 3D Chip

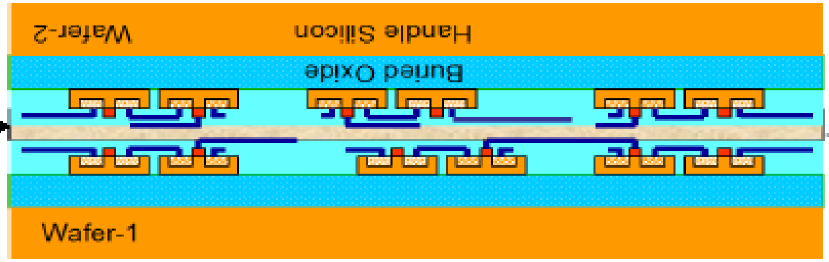
- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - *SOI simplifies via formation*
- Single vendor processing

1) Fabricate individual tiers



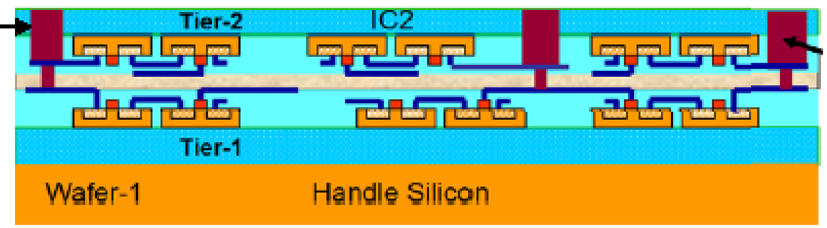
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

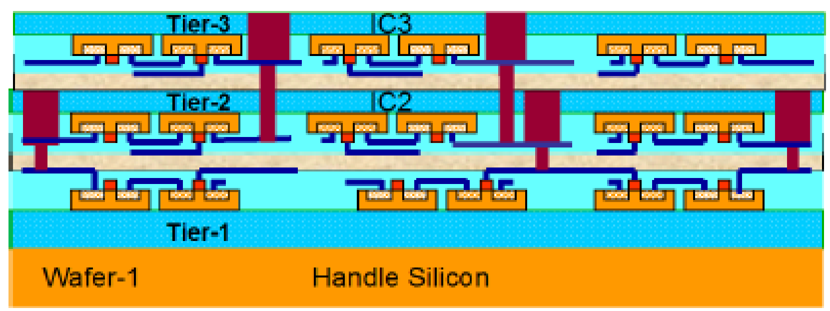


3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Goals for NSLS-II Detector Development

A 'monolithic' photon-counting pixel detector

- 3D version of Pilatus
  - Smaller pixels
  - Better yield

A pixelated detector with spectrum-per-pixel

- Simultaneous spectroscopy/diffraction detector
- energy and spatial resolution
- Laue diffraction
- x-ray microprobes with microdiffraction and fluorescence analysis on the same sample position with the same detector

A pixel detector with multiple-tau time autocorrelation electronics on each pixel

- megapixel detector with on-pixel correlators can provide sufficient sampling density to access the sub-microsecond domain
- 3D technology will provide the necessary integration density

Acknowledgements

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